THE
TOM SWIFT TERMINAL
or,
A CONVIVIAL CYBERNETIC DEVICE

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ACKNOWLEDGMENT

Much is owed to Don Lancaster of Synergetics for stimulating the thinking which led to this design. Both his breakthrough in conceptualizing and realizing the "TV Typewriter", which has stirred such interest in the world of electronic experimentation, and his decision to use random-access memory for the kit version of that device (still in design at this writing) were leaps of applied imagination upon which we have been trying to build.

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NOTE - "Teletype" is a registered trade mark of the Teletype Corporation.

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1. PURPOSE

The purposes of this design are as follows (not necessarily in order of importance);

(a) to provide an inexpensive computer terminal useable in public-access information systems which is;

1. capable of using the home TV set as a character display with hard copy as an add-on option

2. easily useable by untrained people in a non-professional environment

3. readily expandable by field modifications to higher levels of "intelligence" and off-line capability.

(b) to provide a cybernetic building block which is;

1. capable of supporting any one of several integrated-circuit microprocessors as an inependently accessible and manipulable memory

2. capable of extensive modification and adaptation through the addition of plug-in modules designed and built by the user or third parties

3. sufficiently straightforward in design and operation as to approach the status of a cybernetic educational toy.

(c) to formulate, examine, and test principles of "convivial" design and manufacture as suggested by Ivan Illich (Tools For Conviviality).

2. APPROACH

a. CONVIVIALITY

Is the usefulness of a technology to people in direct proportion to its complexity?

Ivan Illich, writing in Tools for Conviviality, argues that not only is the social utility of technology not directly related to its complexity, but that increasing complexity may bring about decreasing social usefulness.

While the function performed by the technological device may be faster, more accurate, more "efficient" on a short-run basis, Illich argues, the instituions of specialistsrestricted access, "black box" non-repairable components, mystification and fragmentation of understanding which accompany the new tool usually negate most of the anticipated benefits of the device.

But is this symbiosis of tool and institution inevitable? Illich believes that it is not. He points out that technological tools and systems can be made "convivial" (as opposed to "industrial") in design so that the principles of operation and use are visible and can be understood, and the circumstances of operation are not built into the design but are subject to the ingenuity of the user.

We believe that even cybernetic electronics, held by some to be the epitome of mystifying technology, will yield to the application of convivial design. We have heard the industry jokes about the maintenance specialists who are shipped with large computer systems and know that not only are such jokes very nearly true, but that such subordination of man to machine signifies a potentially disastrous tendency of technological development.

In the hopes of trying out some initial convivial design criteria, we are designing this device with the following qualities in mind;

1. Its use is not severely restricted by the design, but is rather "open ended" with expandability possible in several dimensions.

2. It is field-repairable without the need for specialized test equipment.

3. Its operation is "in the open", with a minimum of "black box" components, and can be understood by astute amateur electronics enthusiasts with the help of documentation which accompanies the device.

4. All options mentioned in the following descriptions may be put into effect in the field, by rewiring of certain areas on the circuit cards and/or insertion or removal of readily available integrated circuits. In no case will it be necessary to throw away or return an obsolete section of the device.

It should be noted that taking such criteria into account along with most of the standard industrial criteria (interchangeability of parts, simplicity of assembly and adjustment, low prime cost) results in a product which may not be competitive with devices which do not apply these criteria.

While we expect to offset much of this additional cost through the application of "convivial production" techniques such as labor intensivity, co-operative capitalization, and controlled growth, we have no assurance that this device can "compete" with existing devices on a single-useage, short-term basis.

We therefore ask that the prospective user "think ahead" while considering the following descriptions and take into account the future flexibilities of the device. While it may not be suitable for all cybernetic applications, we feel that there are enough real and potential consumer, educational, and "non-industrial" uses for this device to make its consideration worth while.

We expect to provide users with a continuing documentation service clearly describing the finer points of the device as such points come up. We will serve as a clearing house for applications notes, service and modification tips which users send us. We are highly interested in encouraging creative dialog among users and prospective users which will tend to advance the state of the art.

b. THE BUS SYSTEM

One of the most important features of this device is the fact that data transfer between its various sections is carried out through a "bus system". This will probably require some explanation for those not familiar with state-of-the-art computer design.

In electrical terminology, a bus is a wire which is connected in common to a number of different devices. Usually the term descibes power distribution systems within a complex system. A non-bus power system would have separate power supplies attached to each device in the system; a bus system would have a single power supply connected to many different devices through a single wire, the "power bus".

Recently, the bus concept has been applied to data signal distribution within cybernetic devices. Classically, computer designs have revolved around a centralized processor unit, or CPU, which controls all occurences within the system. All data and control channels radiate from the CPU, and are separate from each other. Thus, data exchanged with the input/output section (I/O) of the computer travels along different channels from data exchanged with the memory section.

The bus-organized computer, as pioneered by Digital Equipment Corporation, radically reduces the degree of centralization of the system. Rather than routing all data transfers through the CPU, all internal data transfers are carried out through a shared data channel, the data bus, under control of a "bus controller" to which all devices are connected.

Confusion is eliminated by assigning each possible data source or destination a number, called an address. A certain range of address numbers correspond to memory storage locations, another much smaller range corresponds to control buffers or "registers" within the CPU or various I/O devices. Every device has the capability of sending data to or requesting data from any of the full range of addresses, subject only to priority assignments from the bus controller.

Thus, the classical design may be considered analogous to a bureaucratic social system and the bus design to a system of free interchange subject only to simple traffic rules.

Physically, the data bus takes the form of a parallel series of wires which tie together a number of connectors. Various devices, usually built on printed-circuit cards, can be plugged into these connectors and gain access to the bus.

It is important to note that in most cases the insertion of a new device on the bus requires that only one or two wires be cut for "series connection"; the majority of the wires accept "parallel connection" without having to disturb the bus. Thus, expansion of a bus-organized computer system is vastly simpler than of a classically-organized one, where redesign is often necessary for expansion.

Most display terminals are designed in a classical fashion in which expandability is not a criterion. Since we wish our device to have a future as much more than a display terminal, we have designed it around a bus interconnection system which is both simple and useful.

Priorities for the exchange of data within the device are set by the user when the system is assembled. A series of wires with push-on connectors is used to interconnect certain terminals of each device within the system. The order of interconnection determines the priority of access to the bus which each device has. Devices "upstream" on this chain have priority over those "downstream". The circuitry to effect this priority is on each device's card; no central bus controller is required for this kind of simple system.

GLOSSARY

a brief description of some of the terms used in this discussion

Scan Line - one line of light generated by the TV screen as its beam sweeps from left to right

Field - 256 scan lines spaced evenly down the screen

Horizontal sync signal - the signal which instructs the TV set to return its beam to the left hand side of the screen and begin a new scan line

Vertical sync signal - the signal which instructs the TV set to return its beam to the top of the screen and begin a new field.

Composite Video - the signal fed to the TV set which includes horizontal and vertical sync signals as well as information about the variations in brightness of the beam as it sweeps through each scan line.

Modulated RF - composite video "carried" by a high frequency signal which simulates the broadcast TV signal and which can successfully enter the antenna terminals of the TV set

Data Line - a line of 32 alphanumeric characters or spaces displayed on the screen.

Cursor - a solid underscore which may appear under any character location on the screen. In the basic system the cursor always appears under the location where the next character will appear.

ASCII - American Standard Code for Information Interchange; a code which relates 96 displayed characters (64 without lower case) and 32 non-displayed control characters to a sequence of 7 "on" or "off" choices.

Modem - (MOdulator/DEModulator) - a device which translates "on" or "off" signals such as are used in ASCII into tones which can be transmitted by audio channels such as the telephone system, and which performs the reverse function at the other end of the channel.

Full/Half Duplex - Full duplex operation allows simultaneous reception and transmission of different data. Half duplex prevents reception during transmission and causes the display of exactly what is transmitted at the transmitting location.

Microprocessor - a small device, usually an integrated circuit "chip", which performs the computational functions of a computer. It usually contains no memory capability and must rely on external circuitry to transfer data to and from outside devices.

c. THE BASIC SYSTEM

The initial conception of this device was as a computer terminal capable of replacing Teletype units and having future possibilites for different levels of editing capabilities. We will refer to the "basic system", as the lowest of these levels - the minimal hardware configuration necessary for operation as a computer terminal.

The basic system is designed to provide a signal to a standard, unmodified television receiver which will produce a display of 32 characters wide by 16 lines deep. A solid underscore, the cursor, indicates where the next character will be positioned on the screen. The cursor automatically advances to the next line after a character is placed at the last location of a line.

A carriage-return character causes a similar advance to the beginning of the next line, but a solid block is displayed at the carriage return location. This is so that data in any line length may be displayed without confusion as to the intended end of line.

A Teletype-format keyboard is included, capable of generating 64 visible characters and 32 "control" characters. Of the control characters, only the carriage return is displayed and stored. Other control characters perform various functions for the system. They are listed below along with their effects;

CR	carriage return	Stores CR in current memory location, advances cursor to first space of next line, stores spaces in intermediate locations, rolls display up one line if previous line was last on screen.
BS	back space	Moves cursor back one location, inhibits display of character at that location.
LF	line feed	If immediately following CR, ignored. Otherwise, advances cursor to same location of next line and fills intermediate locations with spaces. Rolls display up one line if line was last on screen.
US	up space	Rolls display down one line.
BEL	bell	Triggers audible alarm in keyboard.

The basic system has enough memory storage for two screens full of characters (1024 words of 7 bits). Thus, up to 16 lines which have rolled up off screen may be retrieved by the US command.

The keyboard connects to the input card, which plugs into the device "main frame". The input card also has a standard Dataphone connector to which any EIA standard data set or acoustical telephone coupler (modem) may be connected. Full or half duplex operation may be selected by a switch on or off the card.

Data may be entered to the system either in asynchronous serial ASCII format or in parallel 8-bit TTL logic-level format. Thus, various external data transmission sources may be connected to the system by

the user. For instance, receivers and converters using the Baudot code for radio-teletype operation may be designed and attached via the parallel data terminals.

The data rate for serial asynchronous data transmission and reception is switchable between two speeds, each of which is adjustable between 110 and 1200 bits per second (baud).

The display may be synchronized to an external video source. This will allow the mixing of external video with the alphanumerics generated by the terminal.

The basic system therefore consists of the mainframe, power supplies, keyboard and housing, one input card, one 1024 x 7 memory card, and one display card.

(Definition of some of the terms used in the following description of operation may require reference to the glossary.)

During data lines, the display card continuously reads sequences of 32 characters from memory. Each sequence of 32 characters is repeatedly read seven times, once for each scan line of that data line. Since characters are displayed as a matrix of dots 5 wide by 7 deep, each scan line represents one of these 7 horizontal lines of dots for all the characters in that data line.

The speed of the memory is such that it is fully occupied during the time when it is presenting characters to the display card. There is time on the margins of each scan line and during the blank scan lines which separate each data line during which the memory is not being read by the display card.

During these times the memory can refresh itself (a process which requires the equivalent of half a scan line and which may be performed piecemeal, but which must be repeated more often than every 30 scan lines), or other sections within the system may make use of the memory. Characters being inserted into memory must wait for these non-display times. Output devices such as printers which may be attached to the system will have to extract their data during these times.

Fortunately, this waiting requirement will not cause any real conflicts within the basic system, since the screen display is carried out much faster than any other use of memory. The fastest modems in use would present only ten characters to the memory in each field, and there are almost 10,000 available opportunities for memory entry in each field.

A few of these opportunities are used at the beginning of each field for internal data transfers. At these times, the display card updates its information on the first and last memory addresses to be displayed, as well as the position of the cursor. This information is transferred over the same bus as the display data. The display card reads the data from several special memory locations which respond to addresses among the sixteen highest possible address numbers.

These memory locations are not contained in any memory card, but rather represent temporary storage areas or "registers" in the input card. The input card pays attention to the contents of these registers as does the display card. An external device can enter new data into them through the bus and thus change the operating conditions of the system. For example, a printer could change the contents of the cursor register to indicate the character being printed. The display card would automatically locate the cursor at the new position under the character in question. Or an external device might advance the end-of-screen register by one character line, in which case the input card would adjust the beginning-of-screen register's contents to keep no more than 16 lines on the screen.

This capability for external manipulation of the system's parameters is one of the most important features of the device. It means that the intelligence of the system is readily expandable without extensive modification. Ultimately a microprocessor can be plugged into the bus and the system will become a computer.

d. DIMENSIONS OF EXPANDABILITY

In addition to the bus structure described above, the major difference between standard display terminals and this device is the use of random-access memory (RAM), which makes simplified expansion possible.

Classically, display terminals of the video type store their screen's worth of data in a shift register memory. Such shift registers are cheap and effective ways of storing data, but they have serious limitations for other than display terminal operation.

The primary such disadvantage is that data must be retrieved from a shift register in exactly the same order in which it was inserted. There is no way to pick and choose which character you take out of the shift register; it presents the next character in the sequence each time the "clock" signal is triggered.

Random-access memory, on the other hand, enables the device to put and take data anywhere in the memory, without waiting for the entire contents of the memory to parade by. For simple display terminal operation, such flexibility is unnecessary, since data is always displayed in the same order in which it is received.

Where the device can be expected to grow more complex, RAM becomes an advantage. Any section in the device can alter or read the data in the memory which concerns that section as soon as it has priority. This is necessary for the opration of microprocessors, which make continuous use of memory and run only slightly slower than the fastest part of the basic system, the display card.

Memory is expandable in size, first to 8 bits per word (7 bit words are provided with the basic system), and then in increments of 1024 words up to 16,000 words. Using memory cards of 4096 words each, the memory may be expanded to over 65,000 words.

Memory may be speeded up, at a corresponding increase in cost. MOS semiconductor memory is available commercially in speeds up to 100 nanosecond cycle time (0.1 microsecond, a factor of ten faster than the basic system memory). Higher speed memory will be necessary if 72 or 80 character lines are desired on a CRT display.

We intend to develop a small dot-matrix line printer which can plug into the bus and print out either the entire contents of memory or single lines as they roll up off the screen, or the displayed characters on the screen. As the editing capabilities and "intelligence" of the device are increased, the printer will be able to print selected fields or blocks within the memory.

The direction of our development for public-access information systems indicates that we will soon require a microprocessor to handle advanced off-line editing and parsing. The device is being designed with this expansion in mind, and even the basic system can accept any of several available microprocessors on its bus.

Programmable-read-only-memory cards will be easily built for use on the bus; such memories are used with microprocessors to allow storage of programs when power is off.

An option on the display card of the basic system will allow the display of memory data as binary, rather than as ASCII characters. The space where each character had been displayed would then appear as a stack of horizontal lines, some solid, some broken. The solid lines represent zeroes while the broken lines represent ones. The bottom line will correspond to the least significant data bit and the top line to the most significant.

For 8-bit memory data this will yield a stack of eight lines, looking somewhat like the six-line hexagram used in the I Ching. For this reason we call this type of display "hexagram display".

A device using hexagram display will provide a highly useful tool in developing and testing applications involving microprocessors. The memory is visible and alterable directly, and not dependent on the operation of the microprocessor or debug programs. It will not be necessary to learn the debug, input/output, and assembler programs usually required for using a processor. Thus machine-language programming of a microprocessor can move into more visual realms using this device and raises the prospect that children and other non-specialists can gain a mastery of computers through it.

This device can also be used to test microprocessors, reducing what might be complex interactions to visible patterns of failure.

For those considering larger systems, we do not see this device as limited to one bus structure. "Bus transceivers" will eventually be available which can carry out two-way high-speed transfers of data between two busses. This makes multiple-bus configurations such as lines, rings, and stars a possibility, and raises interesting prospects for low-cost "distributed-computer" systems.

Other devices which could be attached to the device would include; light pens, "turtles" and "mice", floppy discs, magnetic tape, digital-analog and analog-digital converters, graphic display synthesizers, tone generators, etc.

It is our intention to provide adequate documentation and support to encourage user expansion and modification of this device.

3. REALIZATION

a. MAINFRAME AND BUS

1. BRIEF DESCRIPTION

The mainframe and bus consist of the following components;

1. A physical card cage assembly capable of holding up to 8 circuit cards, each 4.5 by 6.5 inches.
2. Power supplies for 5 and 12 volts DC.
3. In the basic system, 6 44-pin printed-circuit sockets
4. Wiring connecting these sockets as follows;
   (a) data bus - 8 twisted pairs
   (b) address bus - 16 twisted pairs
   (c) +5 volts, -12 volts, ground
5. two terminator cards, which plug into the end sockets.

The physical configuration of the mainframe is as follows;

1. Each card cage occupies a box approximately 7"W x 5"H x 7"D
2. All power supplies are mounted on a plate approximately 7"W x 10"D and stand no more than 5" high.
3. The keyboard consists of a separate unit, approximately 14" wide and no more than 4" high.
4. All the above assemblies mount on a base plate approximately 15 x 15 inches, with carrying handle attached.

OPTIONS - MAINFRAME AND BUS

a. Priority "daisy chain"; a set of wires with push-on connectors for assembling the priority chain. Each card has a priority input and output if it will make memory requests. Priority is established by position of the card on the chain.

b. Up to 2 additional sockets can be added to the card cage. Expansion of the system to up to 24 will be possible if additional card cages are wired together to form an extended bus structure.

c. Base plates for mounting in standard 19-inch racks will be available with or without provision for keyboard.

b. MEMORY

1. BRIEF DESCRIPTION

Memory for the basic system will be provided in the following configuration;

1024 x 7 bits per card

1 microsecond cycle time

Random access, MOS semiconductor, dynamic with on-card refresh circuitry. Refresh occurs during cycles where no prior memory request is made to the card. If refresh does not complete a 32-address cycle within a 1.5 millisecond timeout, an on-card overriding priority is asserted until refresh is completed.

power requirements; 5 volts, -12 volts DC

Inputs;
- address - 10 bits
- card select - 6 bits
- data - 8 bits (bidirectional

Output;
- data - 8 bits(bidirectional)

Control;
- Memory request (in)
- Memory acknowledge (out)
- Write enable (in)
- Clock - 3.58 MHZ - (in)

2. OPTIONS - MEMORY

a. 8 bit word length - insertion of additional memory chip into existing circuit board holes

b. CARD SELECT - rewiring of jumper wires on card selects high-order address bits from which card select signal is derived. NOTE; top address page requires additional protection to prevent interference with the top sixteen words used by registers. Protection circuitry is not provided.

c. DISPLAY

1. BRIEF DESCRIPTION

The functions of the Display Card are as follows;

a. to generate 3.58 MHZ clock, dot clock, character clock, line clock, horizontal and vertical sync signals

b. During each display field, to access sequential memory locations starting with the beginning-of-screen address (provided externally) and continuing to the end-of-screen address (provided externally) and to display the ASCII equivalent of this data on a 5 x 7 dot matrix.

c. At the equivalent memory location given by the Cursor register (provided externally), to display a solid underscore below the data line.

d. To display carriage-return characters (ASCII 015) as solid blocks where they appear.

e. To provide a composite video signal (EIA standard) and a VHF modulated-RF signal carrying this video and timing information.

2. OPTIONS - DISPLAY

a. Suppress CR display - jumper change on card or switch off card

b. Hexagram Display - jumper change on card or switch off card

c. Sync to external signal - jumper changes and chip insertion. allows vertical and horizontal synchronization from external video source.

d. Line length expansion - jumper changes, chip insertion. Allows line legth of up to 40 characters.

d. INPUT

1. BRIEF DESCRIPTION

Input and editing functions are performed by the Input card on the Basic System. The card contains three registers;

a. BOS - beginning of screen; the absolute memory location of the first character to be displayed on the screen.
b. EOS - end of screen; the absolute memory address of the first character beyond which and including which the display is blanked.
c. CRS - Cursor; the absolute memory address at which the next data character entered will be stored.

Each register consists of two eight-bit bytes and responds to two memory addresses in the top sixteen bus addresses. The bus may read or alter the contents of all registers.

The card receives characters either in parallel logic-level format (TTL levels) or in serial asynchronous EIA format (RS-232B). Incoming characters are assumed to be in ASCII code.

All display control is performed by manipulating the contents of the three registers mentioned above. The following is a list of control codes and their effects;

CR Carriage Return - Stores CR in memory, stores spaces in succeeding locations until CRS equals address corresponding to the beginning of the next line.

LF Line Feed - Stores spaces in current and succeeding 31 locations. Ignored if immediately following CR.

BS Back Space - Decrements CRS by one

US Space up - Decrements BOS by 32. Decrements CRS to BOS plus 512 if greater than that number.

BEL Bell - Sets "Alarm" control line active for one second.

DC1 Clear Screen - Sets CRS equal to BOS

DC2 Clear Screen and Home - sets CRS and BOS equal to zero.

EOS is at all times maintained equal to CRS.

CRS is always incremented by one after a character is stored.

Unless US has been received, BOS is incremented by 32 whenever CRS is greater than BOS plus 512.

2. OPTIONS - INPUT

a. Suppress CR store - jumper change. Prevents CR from being entered into memory

b. Alternate Baud Rate - external switch. Enables alternately adjustable baud rate of 110 to 1200.

c. Suppress Control - external switch. Enables acceptance of binary characters which might otherwise simulate control characters.